CWD LIMITED

Datasheet

CBTMN32

An nRF52832 based multiprotocol ultra-low power BLE module

Table of Contents

1. General Description

CBTMN32 is a multiprotocol module that supports Bluetooth 5.3 stack for BLE (Bluetooth Low Energy) and is designed for high data rate short-range wireless communication in the 2.4GHz ISM band. Further the module supports SIGMESH protocol and ANT protocol.

The module is based on Nordic Semiconductor chipset NRF52832 radio transceiver IC that has a 32bit ARM Cortex-M4F CPU, Flash memory and analogue and digital peripherals. The CBTMN32 module provides a low power and ultra-low-cost solution for wireless transmission applications. The module also supports NFC-A tag interface for OOB pairing.

2. Applications

Due to varied support of protocols and stacks, the CBTMN32 module can support varied applications. A brief of the applications is as below:

- Computer peripherals and I/O devices like Mouse, Keyboard, Multi-touch Trackpad
- Interactive entertainment devices like Remote control, 3D Glasses and Gaming Controller
- Use in Personal Area Networks like Health/Fitness Monitor Devices, Medical Devices, Key-Fobs and Wrist Watches
- Remote control toys
- Beacons
- Bluetooth Gateway
- Indoor usage like Home Appliances, Mesh-Controlled Lighting Systems, Color Control for LED Lighting

3. Features

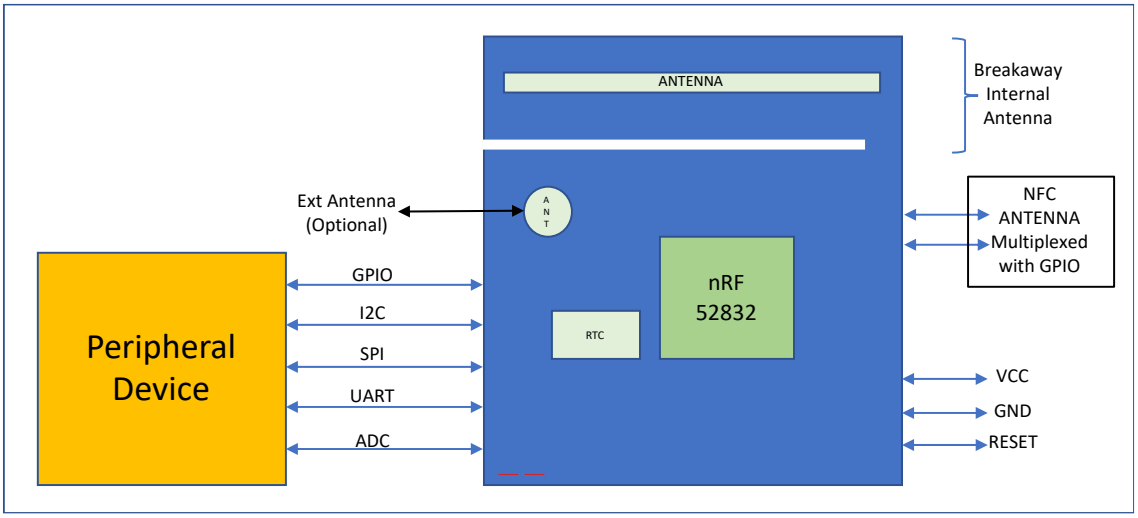
2.4 GHz transceiver	• -96 dBm sensitivity in Bluetooth® low energy mode • Supported data rates: 1 Mbps, 2 Mbps Bluetooth® low energy mode • -20 to +4 dBm TX power, configurable in 4 dB steps • On-chip balun (single-ended RF) • 5.3 mA peak current in TX (0 dBm) • 5.4 mA peak current in RX • RSSI (1 dB resolution)
ARM® Cortex®-M4 32-bit processor with FPU, 64 MHz	• 215 EEMBC CoreMark® score running from flash memory • 58 µA/MHz running from flash memory • 51.6 µA/MHz running from RAM • Data watchpoint and trace (DWT), embedded trace macrocell (ETM), and instrumentation trace microcell (ITM)

	• Serial wire debug (SWD) • Trace port
Flexible power management	• 1.7 V–3.6 V supply voltage range • Fully automatic LDO and DC/DC regulator system • Fast wake-up using 64 MHz internal oscillator • 0.3 µA at 3 V in System OFF mode • 0.7 µA at 3 V in System OFF mode with full 64 kB RAM retention • 1.9 µA at 3 V in System ON mode, no RAM retention, wake on RTC
Memory	• 512 kB flash/64 kB RAM • 256 kB flash/32 kB RAM
Other features	• Microprocessor Control Unit (MCU): nRF52832 • Nordic SoftDevice ready • Support for concurrent multi-protocol • Type 2 near field communication (NFC-A) tag

	with wakeup-on-field and touch-to-pair capabilities • 12-bit, 200 kSPS ADC - 8 configurable channels with programmable gain • 64 level Comparator • 15 level low power comparator with wakeup from System OFF mode • Temperature sensor • 30 general purpose I/O pins • 3x 4-channel pulse width modulator (PWM) unit with EasyDMA • Digital microphone interface (PDM) • 5x 32-bit timer with counter mode • Up to 3x SPI master/slave with EasyDMA • Up to 2x I2C compatible 2-wire master/slave • I2S with EasyDMA • UART (CTS/RTS) with EasyDMA • Programmable peripheral interconnect (PPI)

	• Quadrature decoder (QDEC) • AES HW encryption with EasyDMA • Autonomous peripheral operation without CPU intervention using PPI and EasyDMA • 3x real-time counter (RTC)

4. Application Block Diagram



5. Interfaces

5.1. Power Supply

Regulated power for the SKB369 is required. The input voltage Vcc range should be 1.7V to 3.6V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

5.2. Function Interfaces

5.2.1. GPIOs

The general purpose I/O is organized as one port with up to 30 I/Os enabling access and control of up to 30 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high- or low-level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals

- All pins can be configured as PWM
- There are 6 ADC/LPCOMP input in the 30 I/Os

5.2.2. Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps, 250kbps and 400 kbps.

5.2.3. Flash Program I/Os

The module has two programmer pins, SWDCLK pin and SWDIO pin respectively. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

5.2.4. Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals.

SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line and can be chosen from any GPIOs on the device and configured independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral supports SPI modes 0,1,2, and 3. The module has 3 SPI ports, and their properties are as below:

Instance	Master / Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

5.2.5. UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported. It supports the following baud rate in bps unit: 1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200.

Note: The GPIOs are used for each SPI/TWI/UART interface line and can be chosen from any GPIOs on the device and configured independently.

5.2.6. Analogue to Digital Converter (ADC)

The 12-bit incremental Analogue to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference pre-scaling, and sample resolution (8,10, and 12 bit).

Note: The ADC module uses the same analogue inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

Module PIN Number	nRF52832 PIN Number	Description
2	P0.2/AIN0	General Purpose I/O SAADC/COMP/LPCOMP input
3	P0.3/AIN1	General Purpose I/O SAADC/COMP/LPCOMP input
4	P0.4/AIN2	General Purpose I/O SAADC/COMP/LPCOMP input
5	P0.5/AIN3	General Purpose I/O SAADC/COMP/LPCOMP input
28	P0.28/AIN4	General Purpose I/O SAADC/COMP/LPCOMP input
29	P0.29/AIN5	General Purpose I/O SAADC/COMP/LPCOMP input
30	P0.30/AIN6	General Purpose I/O SAADC/COMP/LPCOMP input

31	P0.31/AIN7	General Purpose I/O SAADC/COMP/LPCOMP input

5.2.7. Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analogue inputs on the device.

Additionally, the low power comparator can be used as an analogue wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

5.2.8. Reset

The reset pin of the module is in the internal pull-high state. When the reset pin of the module is input to a low level, the module will be automatically reset. After the reset pin is used, the parameters of the current setting will not be ANT.

5.2.9. NFC

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC

Forum. With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

Listed here are the main features for the NFC peripheral:

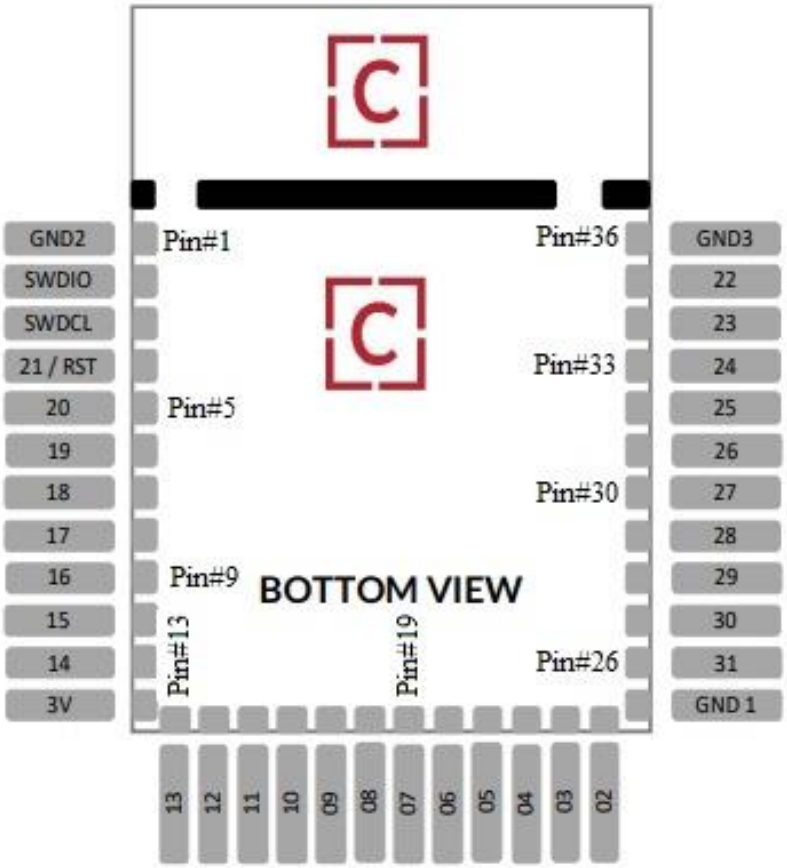
- NFC-A listen mode operation
- 13.56 MHz input frequency
- Bit rate 106 kbps
- Wake-on-field low power field detection (SENSE) mode
- Frames assemble and disassemble for the NFC-A frames specified by the NFC Forum

6. Module Specifications

Hardware Features	
Model	CBTMN32
Antenna Type	PCB Antenna
External RF Switch	MM8130-2600
Chipset Solution	nRF52832
Voltage	1.7v ~ 3.6v
Dimensions (L x W x H)	25.40 x 20.07 x 1.10 mm (With PCB Antenna) 18.44 x 20.07 x 1.10 mm (Without PCB Antenna)
Wireless Features	
Wireless Standards	BLE 5.3, BLE MESH, ANT
Frequency Range	2400MHz-2483.5MHz
Data Rates	1-2Mbps
Wireless Security	AES HW Encryption
Transmit Power	Tx Power -20 to +4 dBm in 4dB Steps
Operating Mode	Central / Peripheral in BLE

7. Module Pin-out and Pin Description

7.1. Module Pin-out



7.2. Pin Description

Sr. No.	CBTMN32 Pins	NRF52832 MCU PIN	PIN DESCRIPTION
36	GND	GND	
35	P0.22	P0.22	General purpose I/O pin
34	P0.23	P0.23	General purpose I/O pin
33	P0.24	P0.24	General purpose I/O pin
32	P0.25	P0.25	General purpose I/O pin
31	P0.26	P0.26	General purpose I/O pin
30	P0.27	P0.27	General purpose I/O pin
29	P0.28	P0.28/AIN4	General purpose I/O pin (SAADC/COMP/LPCOMP)
28	P0.29	P0.29/AIN5	General purpose I/O pin (SAADC/COMP/LPCOMP)
27	P0.30	P0.30/AIN6	General purpose I/O pin (SAADC/COMP/LPCOMP)
26	P0.31	P0.31/AIN7	General purpose I/O pin (SAADC/COMP/LPCOMP)
25	GND	GND	GND
24	P0.02	P0.2/AIN0	General purpose I/O pin (SAADC/COMP/LPCOMP)
23	P0.03	P0.3/AIN1	General purpose I/O pin (SAADC/COMP/LPCOMP)
22	P0.04	P0.4/AIN2	General purpose I/O pin (SAADC/COMP/LPCOMP)

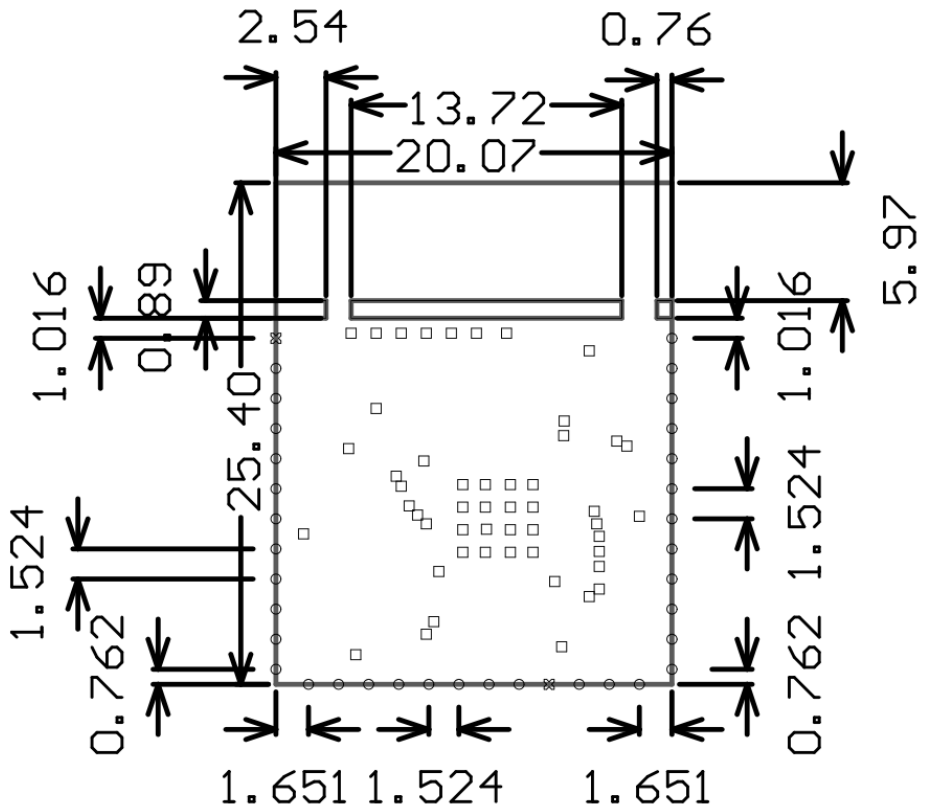
21	P0.05	P0.5/AIN3	General purpose I/O pin (SAADC/COMP/LPCOMP)
20	TX	P0.6	General purpose I/O pin
19	P0.07	P0.7	General purpose I/O pin
18	RX	P0.8	General purpose I/O pin
17	P0.09	P0.9	General purpose I/O pin
16	P0.10	P0.10	General purpose I/O pin
15	P0.11	P0.11	General purpose I/O pin
14	P0.12	P0.12	General purpose I/O pin
13	P0.13	P0.13	General purpose I/O pin
12	3.3V	3.3V	General purpose I/O pin
11	P0.14	P0.14/TRACEDATA [3]	General purpose I/O pin. Trace port output
10	P0.15	P0.14/TRACEDATA [2]	General purpose I/O pin. Trace port output
9	P0.16	P0.14/TRACEDATA [1]	General purpose I/O pin. Trace port output
8	P0.17	P0.17	General purpose I/O pin
7	P0.18	P0.18/TRACEDATA [0]/SWO	General purpose I/O pin. Trace port output. Single wire o/p
6	P0.19	P0.19	General purpose I/O pin
5	P0.20	P0.20/TRACECLK	General purpose I/O pin. Trace port clock output
4	RESET	P0.21/nRESET	General purpose I/O pin. Configurable as pin reset
3	SWCLK	Programming Clock	Serial wire debug clock input for debug and programming

2	SWDIO	Programming Data IN/OUT	Serial wire debug I/O for debug and programming
1	GND	GND	GND

8. PCB Design Guide

Please reserve empty area for PCB Antenna when designing a device's board. The empty range minimum size should be 20.6 x 6.88mm. Do check the "PCB footprint and dimensions" for reference.

9. PCB Footprint and Dimensions



Dimensions: 25.40mm x 20.07mm x 1.10mm

10. Electrical Characteristics

10.1. Absolute Maximum Ratings

Parameter	Condition	Min.	Typical	Max.	Unit
Storage Temperature		-40		125	℃
ESD Protection	VESD			4000	V
Supply Voltage	VCC	-0.3		3.9	V
Voltage on Any I/O Pin		-0.3		3.63	V

10.2. Recommended Operating Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Temperature	TA	-40	25	85	℃
Power Supply	VCC	1.7	3.3	3.6	V
Input Low Voltage	VIL	0		0.3xVC	V
Input High Voltage	VIH	0.7xVC		VCC	V

10.3. Current Ratings

System State	TX Peak @ 4dBm	RX Peak	Sleep Mode (Average)	Idle Mode (Average)
Current (peak) @ 3V	7.5mA	5.4 mA	0.4 uA	1.2 uA

11. Ordering Information

Module No.	Shielding	Antenna
CBTMN32	No	PCB Antenna

12. Contact Information

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